MANCHESTER 1824

The University of Manchester

INTRODUCTION

- Managed runtime systems dominate user-friendly programming languages
- **RISC-V J-Extension Working Group is focused on** providing extensions for managed, interpreted and JIT-ed languages
- Currently the only JVM capable of executing (some) Java workloads on RISC-V is JikesRVM
- More VMs are needed to explore optimizations and evaluate their impact

MAXINE VM

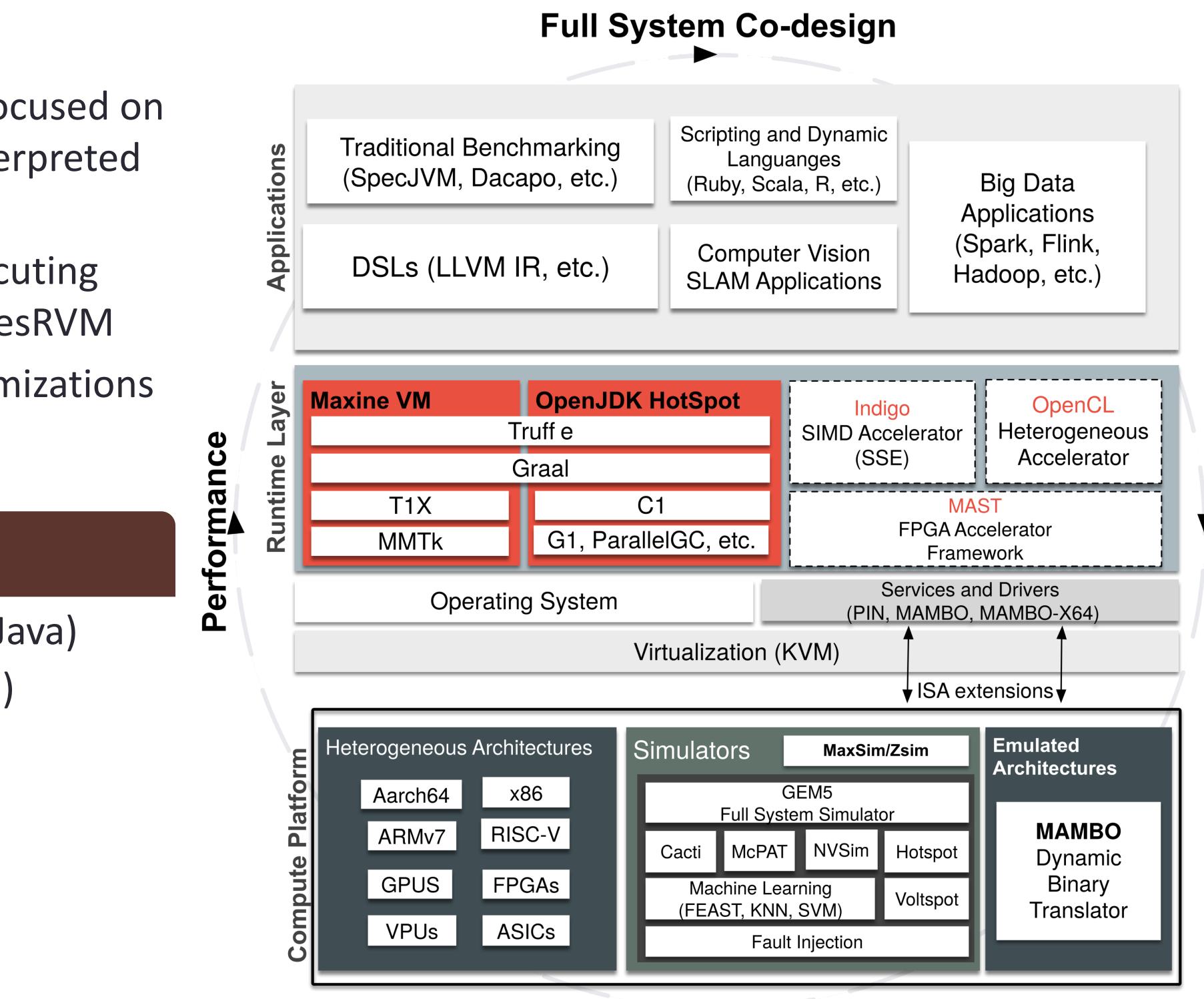
- Meta-circular VM (Java VM written in Java)
- Multiple JIT compilers (T1X, C1X, Graal)
 - JVMCI Compatibility
- Multiple GC algorithms
 - MMTk Integration
- Multiple ISAs
 - X86_64, ARMv7, Aarch64
- Cross-ISA testing framework [1]
 - Allow porting of compilers on new ISAs through cross-compilation and simulation
- Integration with ZSim in MaxSim [2]
- Part of the Beehive ecosystem [3]

[1] C. Kotselidis, A. Nisbet, F. S. Zakkak, N. Foutris. Cross-ISA debugging in meta-circular VMs. In VMIL 2017.

- [2] A. Rodchenko, C. Kotselidis, A. Nisbet, A. Pop, M. Lujan. MaxSim: A simulation platform for managed applications. In ISPASS 2017.
- [3] C. Kotselidis, J. Clarkson, A. Rodchenko, A.Nisbet, J. Mawer, M. Luján. Heterogeneous Managed Runtime Systems: A Computer Vision Case Study. In VEE 2017.

Enabling RISC-V support on MaxineVM Foivos Zakkak, Juan Fumero and Christos Kotselidis first.last@manchester.ac.uk

THE BEEHIVE ECOSYSTEM



Resiliency

Beehive Characteristics:

- Modular and easily extensible
- Implemented with high-level languages with good IDE support and low entry-barrier
- Realistic and diverse simulation infrastructures
- Support of multiple hardware architectures
- Support of heterogeneous systems
- Capability of implementing multiple languages
- Integration with popular research tools





MAXINE VM	
 Ported Cross-I 	
 Created RISC- 	
 Active assemb)
JUNIT Testing Frame	
Initializer	
AssemblerTeste	
T1XTester	
C1XTester	
Q	
riscv64-unknown-elf- mcmodel=medany -fvis Ttest_riscv64.ld sta	5
qemu-system-riscv64	
1. 2. 3.	

CONTACT

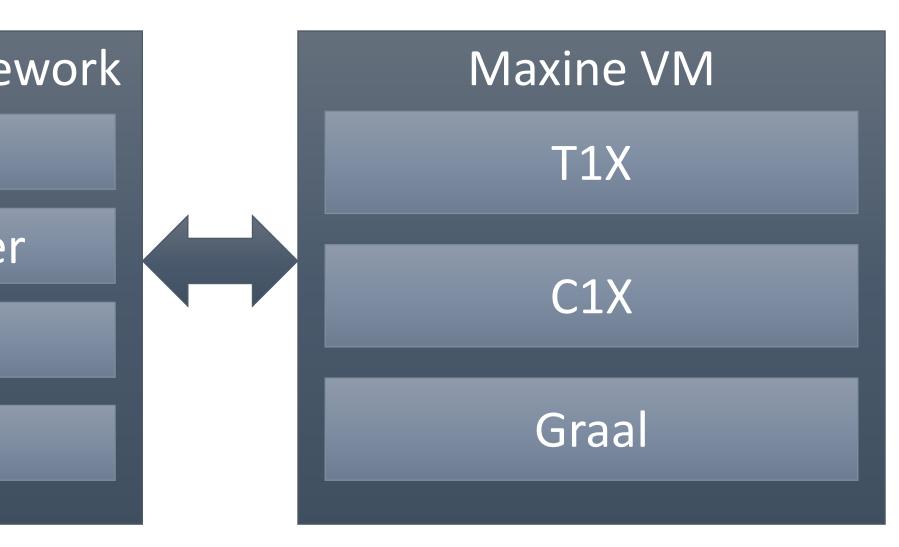
All software is open-source: https://github.com/beehive-lab

We welcome external contributions! Please contact: christos.kotselidis@manchester.ac.uk



RISC-V STATUS

ISA Testing Framework V Assembler Skeleton bler development



EMU & GCC Toolchain

Binary Creation

-gcc -g -march=rv64g -mabi=lp64d -static sibility=hidden -nostdlib -nostartfiles artup_riscv64.s test_riscv64.c -o test.elf

Simulated Execution

-M virt -m 128M -kernel -s -S test.elf

Validate Results

Inspect state through GDB Validate state Return PASS/FAIL to Tester

